A 12-Bit Pipelined ADC Design in 0.18 µm CMOS Technology

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ABSTRACT

It is necessaries for many of applications to insist have the best performance of data converters. Data converters with maximum gain of sampling frequency, its resolutions and minimum power consumption is challenging. Data converter with best performance also required for advance electronic technology like communication side application, wideband receivers and many digital devices. This work is to design the structure of data converter Pipeline ADC in low power consumption, with maximum resolution and high speed. Here the 12-bit resolution of pipeline ADC with cascaded stages is designed using the technology of 180nm. The basic part in ADC architecture is operational amplifier. Design architecture of pipeline converter and Op-amp simulate in one volt (1) of given voltage and having sampling frequency is 1.25MHz. The ADC has SNDR of 69.3 dB and having ENOB of 11.2 bits.

Keywords: ADC, SHA, MDAC, VLSI, DAC

1. INTRODUCTION:

Architecture of converters (ADC) are the required parts for analog and mixed signal system. It communicate the analog information with digital one. As the large scale performance of digital information and the processing of signal in communications side, in industrial control, and image processing, the conversion system in this field is fill out excessively. In this advance period of technology, the electronic systems depend to digitized. Universally the use of digital technology are necessary. Information around us in environment is in analog form, like given voltage, current, temperature, pressure, time and many others. The fundamental cause to digitize the input in electronic systems is to minimize the noise consideration, for fastness and solid anti-interference. Advance technology in electronics side use the large-scale integration VLSI for achieving the lower power consumption and for higher speed with many characteristics and cheap cost. This architecture of 12-bit pipeline ADC that utilize 1-V supply voltage are design in 180nm CMOS technology. Figure 1 shows the detail structure of pipeline ADC. Sample-and-hold (SHA) amplifier is essential part in ADC architecture for best performance on output. Section A describe with detail of S/H and B with detail of MDAC

In section, 2 the basic block of operational amplifier used in ADC presented. A pipeline ADC consist of cascaded stages. In this design, all stages have the cascaded structure, which describe in section 3. The measurement result is given in part 4 and conclusion in part 5. References gives with detail in last section 6.

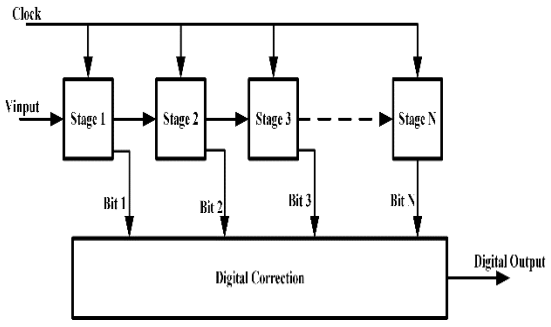

Fig.1 Complete Pipeline Structure.

A. Sample and Hold (S/H)

The sample and hold circuit is commonly used for such analog signal to digital interface in the beginning of converter [3]. In our performance, the broadband

and less distortion, with maximum linearity of sample-and-hold circuit is required. The typical 2-capacitor flip around the architecture of sample and hold. The sample and hold circuit assists for receiving to best performance with minimum power consumption. The pipeline ADC have must the SHA which hold the input signal, whenever the next operation are completed. During sample stage, input signal is sampled in parallel on two equally sized capacitor [9]. SHA schematic is given in Fig. 2.

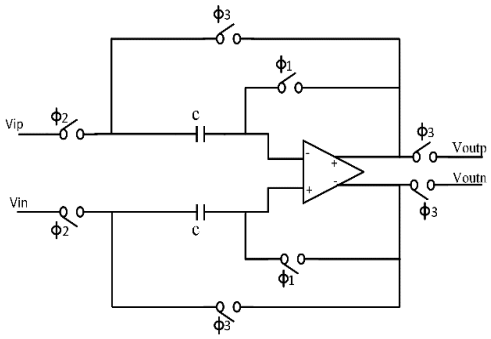

Fig. 2. Structure of SHA

B. MDAC

MDAC is a critical block performing multiple jobs such as signal subtraction, multiplication and the SHA function. The sampling capacitance sampled the given input signal in MDAC architecture [1]. Bit stream then goes through a 1.5-Bit DAC to create 1.5-Bit analog signal. This 1.5-bit DAC makes the transition from the digital codes (one or zero) to the analog domain. All the performance of MDAC architecture like speed and low noise stability depend upon the performance of operational amplifier used in MDAC architecture. Circuit diagram of MDAC is given in diagram of figure 3.

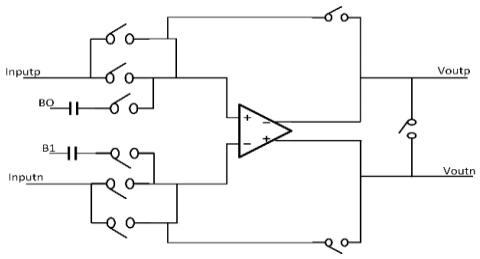

Fig.3 Complete MDAC Structure.

2. OP-AMP BLOCK

The operational amplifier is the main basic block in pipeline architecture. The residue gain provided by operational amplifier to the system. Converter are fully dependent on best performance of operational amplifier like slew rate and bandwidth, which is used in both sample, and hold schematic and MDAC. The maximum load of capacitance in the beginning stage have maximum settling errors, while in next part then op-amp can operate very fast because of low capacitive loading. The amplifier is scaled down once and use in all the remaining stages without further scaling [2]-[5]. Symbol of op-amp is given in figure 4.

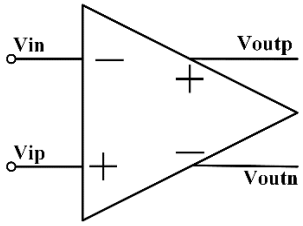

Fig. 4. Symbol of Operational Amplifier

3. ADC STAGES STRUCTURE

ADC architecture work on consecutive stages and each stage has same structure except the 1st one, and the last block is 2-Bit Flash ADC. 1st stage have the circuit of SHA, 1.5-bit ADC converter, DAC, Adder and Residue amplifier that includes an inter-stage amplifier to provide gain. All stages designed with Sample and Hold except the 1st one. At any given time, the (1st) stage utilize the fresh coming samples

while the other operates on residue from last stages samples. To convert the digital output of ADC converter back in analog we us the block of sub-DAC. This approximate the analog signal subtract from given input signal.

The execution of pipeline converter is based on bit per stages. For less consumption of power, the beginning stage settle the number of bits necessaries to minimize the noise restriction of the stages to a level that can be played with minimum size of sampling capacitor [8].

********* The balanced signal is send to the next stage for processing and the current stage start process for incoming signal [4]. Complete structure of pipeline ADC is given in figure 4.

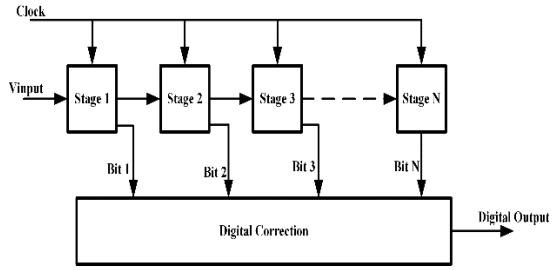

Fig 5. Complete Structure of pipeline ADC

The digital data from stages then received by digital correction area of converter and set them with proper delay. During digital processing technique the digital code are processed in digital domain and give the information in clarity to analog circuit [10].

Output of 12-bits of data, the two least significant digits are used for calibration and are abbreviated the final conversion result [6]. The mention work is based on 1.5-bit cascaded stages and the detail schematic of first stage is given in fig.6 with detail.

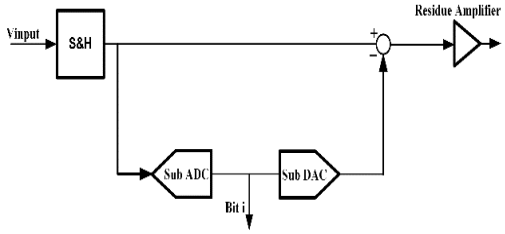

Fig 6. Pipeline stage structure

4. MEASUREMENT RESULT

The proposed ADC architecture design in 180nm CMOS technology. Have occupy the small die area with low supply voltage of 1-V and have the sampling frequency of 1.25 MHz. Output wave form result is given in figure 6.

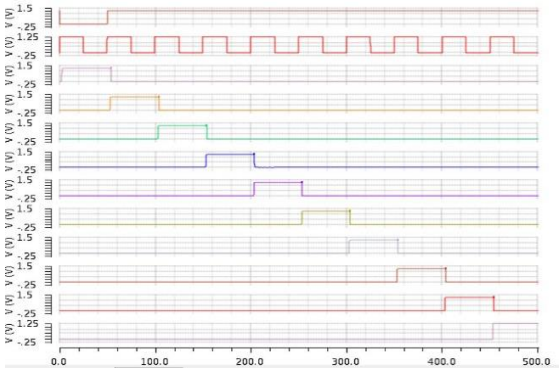

Fig 6. Structure output wave form

5. CONCLUSION

This work present a 12 bit of 1.25 Mega sample frequency per second pipeline converter with digital calibration. Low power Op-amp with suitable gain is the main function block of ADC. Best performance ADC with digital output is given in paper with the scaling of supplies and transistor dimension.

6. REFERENCES

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